LISTING OF AND AMENDMENTS TO CLAIMS:

1. (canceled)

2. (currently amended) A method as recited in claim 40 [[1]], further comprising:

supplying an interrupt from the peripheral devices to the processor when the processor changes activity states from a first activity state to a second activity state.

3. (currently amended) A method as recited in claim 2, further comprising detection of the activity state of the processor by the peripheral devices before said interrupt is supplied.

4. (canceled)

5. (currently amended) A method as recited in claim 2, wherein the peripheral devices have has a plurality of urgency states and an activity state of the processor is evaluated against an [[the]] urgency state of a [[the]] peripheral device to determine whether said peripheral device issues an interrupt.

6. (canceled)

7. (currently amended) A method as recited in claim 5, wherein if said urgency state of a said peripheral device is low, said peripheral device issues an interrupt to said processor only if said activity state of said processor is other than low.

8.   (canceled).

9.   (canceled).

10.   (currently amended)   A method as recited in claim 40 [[8]], further comprising setting the urgency level of each of the peripherals that have been serviced to a lowest urgency level after the peripheral has been serviced.

11.   (currently amended) A method as recited in claim 40 [[1]], wherein the activity states of the processor are represented by at least one bit output of the processor.

12.   (currently amended)   A method as recited in claim 40 [[1]], wherein the activity states of the processor are represented by at least one output word generated by the processor.

13.   (currently amended)   A method as recited in claim 40 [[1]], wherein the activity state of the processor is communicated as being in a state selected from active, idle and sleep.

14.   (canceled).

15.   (currently amended) A system as recited in claim 41 [[14]], further comprising means for supplying an interrupt from the peripheral devices to the processor when the processor changes activity states from a first activity state to a second activity state.

16. (currently amended) A system as recited in claim 15, further comprising detection means associated with the peripheral devices for detecting the activity state of the processor before said interrupt is supplied.

17. (canceled).

18. (currently amended) A system as recited in claim 15, wherein the peripheral devices have has a plurality of urgency states, further comprising means for evaluating an activity state of the processor against an [[the]] urgency state of a [[the]] peripheral device to determine whether said peripheral device issues an interrupt.

19. (canceled).

20. (currently amended) A system as recited in claim 18, wherein if said urgency state of a said peripheral device is low, said peripheral device issues an interrupt to said processor only if said activity state of said processor is other than low.

21. (canceled).

22. (canceled).

23. (currently amended) A system as recited in claim 41 [[21]], further comprising:

    means for setting the urgency level of each of the peripherals that have been serviced to a lowest urgency level after the peripheral has been serviced.

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24. (currently amended) A system as recited in claim **41** [[14]], wherein the activity states of the processor are represented by at least one bit output of the processor.

25. (currently amended) A system as recited in claim **41** [[14]], wherein the activity states of the processor are represented by at least one output word generated by the processor.

26. (currently amended) A system as recited in claim **41** [[14]], wherein the processor has activity states selected from active, idle and sleep.

27. (canceled).

28. (currently amended) A computer program product as recited in claim **42** [[27]], further comprising computer readable program code means embodied therein for causing the computer to supply an interrupt from the peripheral **devices** to the processor, when the processor changes activity states from a first activity state to a second activity state.

29. (currently amended) A computer program product as recited in claim **42** [[21]], further comprising computer readable program code means embodied therein for detecting the activity state of the processor.

30. (canceled).

31. (currently amended) A computer program product as recited in claim 28, wherein the peripheral has a plurality of urgency states, further comprising computer readable program code for evaluating an activity state of the processor against the urgency state of a [[the]] peripheral device, to determine whether said peripheral device issues an interrupt.

32. (canceled).

33. (currently amended) A computer program product as recited in claim 31, wherein if said urgency state of a said peripheral device is low, said peripheral device issues an interrupt to said processor only if said activity state of said processor is other than low.

34. (canceled).

35. (canceled).

36. (currently amended) A computer program product as recited in claim 42 [[34]], further comprising computer readable program code for setting the urgency level of each of the peripherals that have been serviced to a lowest urgency level after the peripheral has been serviced.

37. (currently amended) A computer program product as recited in claim 42 [[27]], comprising computer readable program code wherein the activity states of the processor are represented by at least one bit output of the processor.

38. (currently amended) A computer program product as recited in claim 42 [[27]], further comprising computer readable program code wherein the activity states of the processor are represented by at least one output word generated by the processor.

39. (currently amended) A computer program product as recited in claim 42 [[27]], comprising computer readable program code for detecting the processor state as a state selected from active, idle and sleep.

40. (new) In a computer system having a processor with a plurality of activity states, and a plurality of peripheral devices in operative relation with the processor, wherein each peripheral device has a plurality of urgency states, a method of operating the computer system comprising:

communicating an activity state of the processor to the peripheral devices;

evaluating an activity state of the processor against an urgency state of a peripheral device to determine whether said peripheral device issues an interrupt, wherein if said urgency state of a peripheral device is high, said peripheral device issues an interrupt to said processor regardless of said activity state of said processor;

issuing interrupt requests to said processor from all peripheral devices which need to be serviced, when an interrupt has been issued to said processor by one of said peripheral devices; and

servicing all of said interrupt requests by said processor.

41. (new) A computer system having a processor with a plurality of activity states, and a plurality of peripheral devices in operative relation with the processor, wherein each peripheral device has a plurality of urgency states, the computer system comprising:

means for communicating an activity state of the processor to the peripheral devices;

means for evaluating an activity state of the processor against an urgency state of a peripheral device to determine whether said peripheral device issues an interrupt, wherein if said urgency state of a peripheral device is high, said peripheral device issues an interrupt to said processor regardless of said activity state of said processor; and

means associated with each of said peripheral devices for detecting when an interrupt has been issued to said processor by one of said peripheral devices, and for issuing an interrupt request to said processor if said peripheral device needs to be serviced;

wherein said processor servicing all of said interrupt requests from peripheral devices needing to be serviced.

42. (new) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing the computer to effect a method for operating the computer system to service interrupts from a plurality of peripheral devices in operative relation with a processor having a plurality of activity states, the method comprising:

communicating an activity state of the processor to the peripheral devices;

evaluating an activity state of the processor against an urgency state of a peripheral device to determine whether said peripheral device issues an interrupt, wherein if said urgency state of a peripheral device is high, said peripheral device issues an interrupt to said processor regardless of said activity state of said processor;

issuing interrupt requests to said processor from all peripheral devices which need to be serviced, when an interrupt has been issued to said processor by one of said peripheral devices; and

servicing all of said interrupt requests by said processor.